KLS Gogte Institute of Technology

Department of Information Science & Engineering

**Internal Assessment- II**

Subject: Logic Design Code: 15CS32

Semester: III Max. Marks: 25

Date: 6-10-2016 Duration: 1 Hour

**Note: Answer all 5 questions for 25 Marks.**

1. Explain the basic idea of working of flip flop. [L2, CLO3, PO1]

2. Explain the working of Master slave JK flip flop. [L2, CLO3, PO1]

3. Draw the circuit diagrams of SR and D flip flops and write truth tables. Demonstrate the timing diagram for positive triggered D flip flop [L1, CLO3, PO1]

4. Outline the working of SISO and PIPO. Draw the circuit diagrams 4 bit of SISO and 4 bit PIPO. [L2, CLO3, PO1]

5. Design 7 segment decoder using PLA. [L6, CLO2, PO3]

.

Staff In charge Stream Leader

Prof. S.B.Deshpande Prof. P.S.Upparmani

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